Logo

Description automatically generated**EEDG/CE 6370**

**Due Date**: Sunday October 8, 11:59pm

16

**Design and Analysis of Reconfigurable Systems**

**Homework 4 – Physical design**

**Student Name: Khoa Diep, Dismas Ezechukwu**

**Part I – Design Implementation and timing analysis**

a.) Follow the instructions in the lab sheet and synthesize the design without replacing any LUT in Chip Planner. Report the logic utilization (ALMS), total registers, pins, block memory, DSP blocks and DLLs used from the Analysis & Synthesis report.

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| Marks |
| 2 |
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ALMs: N/A

Total Registers: 76

Total Pins: 241

Block Memory: 0

DSP Blocks: 0

DLLs: 0

b.) Report the same resource utilization from the Fitter report and compare with the values reported with the ones reported in the Analysis & Synthesis report. Do the results match? Yes, no? Explain why.

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| Marks |
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ALMs: 49

Total Registers: 77

Total Pins: 241

Block Memory: 0

DSP Blocks: 0

DLLs: 0

Comparing Analysis/Synthesis vs. Fitter reports, the results do not match. Specifically, the ALMs and total registers do not match. The ALMs don’t match because the synthesis step simply converts HDL code into a gate-level net list and does not know where each gate is mapped to since that’s the job of the fitter. The total registers of the Analysis/Synthesis step is an estimation while the fitter is the actual mapping of the all gates and logic.

c.) Open the Timing analyzer and report the maximum frequency

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d.) Annotate here the 5 longest critical paths from Timing analyzer and annotate here their delay and slack.

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e.) Change the sdc constraint file setting the clock constraint to a period of 2ns (500Mhz) instead of 20ns (50Mhz). Reopen the Timing analyzer and report the 5 longest critical paths and their slack. Compare with the results in d). What did you notice?

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Comparing 20 ns to 2 ns, the data delay did improve, but with the cost of slack becoming positive to negative. When setting clock constaint from 20ns to 2ns, the timing is not met for at least the 5 worse case scenarios. This tradeoff between delay and slack is not advantageous since the circuit will experience timing issues due to the negative slack.

**Part II – Chip Planner**

1. Change back the sdc clock constraint to 20ns. Move the resources explained in the lab sheet (top and bottom left) using the Chip planner and Re-compile the program.

Report the 5 longest critical paths from Timing Analyzer after the replacement. How did this affect the critical path? Compare the results with the original placement results. Explain why.

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| 6 |
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5 critical paths:

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This reduced the slack and increased the delay. Therefore, after replacement, the critical path was affected negatively. This was due to wire delay, since the Registers/LUTs are further apart due to our placement (which causes a general increase in delays).

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After placement, the critical path utilizes two FF/LUTs placed in the chip planner stage.